REMARKS

Reconsideration of this application is respectfully requested in view of the following remarks.

Claims 1-10 are currently pending in the application and subject to examination.

In the Office Action mailed July 1, 2005, claims 1-10 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 4,858,190 to Yamaguchi et al. (hereinafter "Yamaguchi") in view of U.S. Patent No. 5,282,164 to Kawana. The Applicant hereby traverses the rejection, as follows.

Independent claims 1 and 8 are directed to a data input circuit and a semiconductor device, respectively, for converting input serial data to n-bit parallel data and outputting the n-bit parallel data by following an address signal. Claim 1 and 8 recite, in part:

> a data shifting unit including a plurality of columns, and sequentially shifting the input serial data through the plurality of columns; and a selection unit selecting a column among the plurality of columns as an input column by following the address signal, wherein the input serial data is inputted to said data shifting unit through the input column.

Claim 10 is directed to a method of converting input serial data to n-bit parallel data, and outputting the n-bit parallel data by following an address signal. Claim 10 recites, in part:

> selecting a column among a plurality of columns of a data shifting unit as an input column by following the address signal; inputting the input serial data to said data shifting unit through the input column; and shifting the input serial data sequentially through the plurality of columns.

In each of independent claims 1, 8 and 10, in an input circuit for converting input serial data to n-bit parallel data and outputting the n-bit parallel data, a column from among a plurality of columns of a data shifting unit is selected as an input column by following an address signal. The input serial data is inputted to the data shifting unit through the input column, is sequentially shifted through the plurality of columns, and is outputted as the n-bit parallel data by following the address signal. Thus, the present invention provides a novel device and method whereby serial data may be outputted as parallel data from a plurality of columns, to, for example, a corresponding data bus, efficiently and correctly.

The Office Action asserts that it would have been obvious to have shifted the data in the shift register of Yamaguchi into parallel format, in light of the teaching of Kawana, in order to provide an efficient means for transferring data in applications in which a parallel mode is required.

However, the Applicant respectfully submits that although Kawana teaches parallel output, Kawana neither discloses nor suggests a manner whereby the serial transfer configuration of Yamaguchi may be converted to parallel output. Yamaguchi also fails to disclose or suggest any such teaching. As described in the Description of the Related Art section of the subject application, in parallel mode, each of register data must be transmitted to a corresponding data bus efficiently. Neither Yamaguchi nor Kawana, alone or in combination, discloses or suggests a particular device or method for achieving such efficient transfer. The claimed invention, however, provides a device and a method for achieving efficient transfer of n-bit parallel data, from serial data, to, for example, a corresponding data bus.

In particular, the Applicant respectfully submits that neither reference, alone or combined, discloses or suggests at least the combination of a data input circuit for converting input serial data to n-bit parallel data and outputting the n-bit parallel data by following an address signal, in which a data shifting unit includes a plurality of columns, and sequentially shifts the input serial data through the plurality of columns; and a selection unit selects a column among the plurality of columns as an input column by following the address signal, wherein the input serial data is inputted to said data shifting unit through the input column, as recited in claims 1 and 8.

In addition, the Applicant submits none of the cited references, alone or combined, discloses or suggests at least the combination of selecting a column among a plurality of columns of a data shifting unit as an input column by following the address signal; inputting the input serial data to said data shifting unit through the input column; and shifting the input serial data sequentially through the plurality of columns, as recited in claim 10.

For at least this reason, the Applicant respectfully submits that each of independent claims 1, 8 and 10 recites subject matter that is neither disclosed nor suggested by the applied art of record.

Accordingly, the Applicant respectfully submits that independent claims 1, 8 and 10 are patentably distinct over the combination of Yamaguchi and Kawana and are in condition for allowance.

Claims 2-7 and 9 depend from claims 1 and 8, respectively. Thus, claims 2-7 and 9 are allowable for at least the same reasons as claims 1 and 8, as well as for the additional subject matter recited therein.

Applicant respectfully requests withdrawal of the rejections.

Conclusion

For all of the above reasons, it is respectfully submitted that claims 1-10 are in condition for allowance and a Notice of Allowability is earnestly solicited.

Should the Examiner determine that any further action is necessary to place this application into better form, the Examiner is invited to contact the undersigned representative at the telephone number listed below.

In the event this paper is not considered to be timely filed, the Applicant hereby petitions for an appropriate extension of time. The Commissioner is hereby authorized to charge any fee deficiency or credit any overpayment associated with this communication to Deposit Account No. 01-2300 referencing client matter number 100353-00040.

Respectfully submitted,

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